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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,407	06/13/2001	Zhongze Wang	MI22-1670	8493

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,407	WANG, ZHONGZE	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43 and 61-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43 and 61-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the RCE on 17 October 2003. Claims 1-43 and 61-67 are pending; claims 44-60 have been cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9, 11, 12, 16-19, 21, 22, 36-39, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (5,763,922).

Chau discloses a method of forming a transistor device where a silicon-comprising surface of silicon dioxide (402) is exposed to activate nitrogen to convert the silicon-comprising surface (402) to a material comprising silicon and nitrogen (416); the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of 500 watts to 2,000 watts; providing a channel region (230, 270) on one side of the silicon and nitrogen surface (220, 260); forming a plurality of PMOS (250) or NMOS (210) transistor gate structures on a side of the silicon and nitrogen surface (220, 260) opposed to the one side and forming a pair of source and drain regions (216, 256) separated from one another by the channel region (230, 270) (col. 3, line 4 thru col. 6, line 20). Chau further discloses dividing the transistor gate structures into a first group and a second group and forming a mask (508) over the

second group during the exposure step (Fig. 5D; col. 7, lines 33-63). Chau also discloses the plasma as a remote relative to the silicon-comprising surface and the plasma contacting the silicon-comprising surface (col. 6, line 67 thru col. 7, line 3). Chau discloses implanting a dopant into the channel region with a concentration between $1x10^{16}$ atoms/cm^3 to $1x10^{17}$ atoms/cm^3 (col. 5, lines 48-65).

Chau discloses the claimed invention except for exposing the silicon-comprising surface to activated nitrogen for at least about 20 seconds. It would have been obvious to one having ordinary skill in the art at the time invention was made to expose the silicon-comprising surface to activated nitrogen for at least about 20 seconds, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 1-4, 26-31, 33, 34 and 61-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau in view of Kamath et al. (6,436,845).

Chau discloses a method of forming a transistor device where a silicon-comprising surface of silicon dioxide (402) is exposed to activate nitrogen to convert the silicon-comprising surface (402) to a material comprising silicon and nitrogen (416); the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of 500 watts to 2,000 watts; providing a channel region (230, 270) on one side of the silicon and nitrogen surface (220, 260); forming a plurality of PMOS (250) or NMOS (210) transistor gate structures on a side of the silicon and nitrogen surface (220, 260) opposed to the one side and forming a pair of source and

drain regions (216, 256) separated from one another by the channel region (230, 270) (col. 3, line 4 thru col. 6, line 20).

Chau further discloses dividing the transistor gate structures into a first group and a second group and forming a mask (508) over the second group during the exposure step (Fig. 5D; col. 7, lines 33-63). Chau also discloses the plasma as a remote relative to the silicon-comprising surface and the plasma contacting the silicon-comprising surface (col. 6, line 67 thru col. 7, line 3). Chau discloses implanting a dopant into the channel region with a concentration between $1x10^{16}$ atoms/cm^3 to $1x10^{17}$ atoms/cm^3 (col. 5, lines 48-65). Chau does not disclose the activated nitrogen forming a peak concentration of at least 15 atomic %.

Kamath et al. disclose a method of forming a transistor device where nitrogen is activated in a silicon-comprising surface is 10 thick (col. 9, lines 21-25). Kamath et al. further disclose the activated nitrogen having a concentration of about 20 atomic % (col. 5, lines 23-53).

Since Chau and Kamath et al. are both from the same field of endeavor, a method of forming a transistor device, the purpose disclosed by Kamath et al. would have been recognized in the pertinent art of Chau. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau by the activated nitrogen having a concentration of about 20 atomic % as taught by Kamath et al. to reduce tunneling between the transistor gate and the channel region (col. 5, lines 23-53).

Claims 5, 14, 15, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau in view of Kamath et al. as applied to claims 1-4, 6-9, 11, 12, 16-19, 21, 22, 36-39, 41 and 42 above, and further in view of Schindler et al. (5,962,069).

Chau discloses a method of forming a transistor device where a silicon-comprising surface of silicon dioxide (402) is exposed to activate nitrogen to convert the silicon-comprising surface (402) to a material comprising silicon and nitrogen (416); the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of 500 watts to 2,000 watts; providing a channel region (230, 270) on one side of the silicon and nitrogen surface (220, 260); forming a plurality of PMOS (250) or NMOS (210) transistor gate structures on a side of the silicon and nitrogen surface (220, 260) opposed to the one side and forming a pair of source and drain regions (216, 256) separated from one another by the channel region (230, 270) (col. 3, line 4 thru col. 6, line 20).

Chau further discloses dividing the transistor gate structures into a first group and a second group and forming a mask (508) over the second group during the exposure step (Fig. 5D; col. 7, lines 33-63). Chau also discloses the plasma as a remote relative to the silicon-comprising surface and the plasma contacting the silicon-comprising surface (col. 6, line 67 thru col. 7, line 3). Chau discloses implanting a dopant into the channel region with a concentration between $1x10^{16}$ atoms/cm^3 to $1x10^{17}$ atoms/cm^3 (col. 5, lines 48-65). Chau does not disclose annealing the silicon and nitrogen surface

at a temperature of about 900 ^{o}C for a time between 10 seconds and 60 seconds, by rapid thermal processing at a temperature ramp rate of at least 10 ^{o}C/second.

Schindler et al. disclose a method of forming a transistor device where a silicon and nitrogen layer is formed on a substrate. Schindler et al. further disclose annealing the silicon and nitrogen surface at a temperature between 500 ^{o}C and 850 ^{o}C for a time between 5 seconds and 300 seconds, by rapid thermal processing at a temperature ramp rate between 1 ^{o}C/second and 175 ^{o}C/second (col. 10, lines 29-61).

Since Chau and Schindler et al. are both from the same field of endeavor, a method of forming a transistor device, the purpose disclosed by Schindler et al. would have been recognized in the pertinent art of Chau. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau by annealing the silicon and nitrogen surface at a temperature between 500 ^{o}C and 850 ^{o}C for a time between 5 seconds and 300 seconds, by rapid thermal processing at a temperature ramp rate between 1 ^{o}C/second and 175 ^{o}C/second as taught by Schindler et al. to prepared the surface for further processing steps (col. 10, lines 29-61).

Referring to claims 10, 20, 32 and 40, Chau discloses the power in which the plasma is maintained of claims 10, 20, 32, 40 and 57 wherein the power is between 500 watts and 2,00 watts. It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to maintain the plasma at a power between 1,500 watts and 5,00 watts since it has been held that "In

such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Referring to claims 13, 23, 35 and 43, Chau discloses the temperature in which the silicon-comprising surface is maintained of claims 13, 23, 35, 43 and 60 wherein the temperature is 800 ^{o}C. It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to maintain the temperature of the silicon-comprising surface between 25 ^{o}C and 400 ^{o}C since it has been held that "In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Response to Arguments

Applicant's arguments filed 17 October 2003 have been fully considered but they are not persuasive. As stated above, Chau in view of Kamath et al. disclose the method of forming a transistor as described in claims 1, 6, 16, 26, 36 and 60.

In response to the applicant's arguments, the applicant argues that Kamath et al. discloses nitride concentrations greater than 5% adversely affect semiconductor assembly. However, Kamath et al. further disclose the problems with higher nitride

concentrations can be avoided when the surface exposed to the nitridation is thin (col. 10, lines 31-37).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (703) 605-4299. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PEP

AMIR ZARABIAN
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